



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,249	10/27/2003	Valery M. Dubin	42P16681	4353

. 7590 04/22/2005
MICHAEL A. BERNADICOU
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD,
SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER

LE, DUNG ANH

ART UNIT	PAPER NUMBER
----------	--------------

2818

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

14

Office Action Summary	Application No.	Applicant(s)	
	10/695,249	DUBIN ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 18-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

Du

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 10/27/2003 is acceptable.

Election/Restriction

Application's election without traverse of Group II (Claims 1-17) drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application . Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims 18-26.

Applicants are reminded to cancel non-elective claims.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 10/27/2003 and made of record . The references cited on the PTOL 1449 form have been considered.

Specification -

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is

Art Unit: 2818

requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-11, 13 and 15-17 are rejected under 35 USC 102 (b) as being anticipated by Nogami et al. (6,022,808).

Nogami et al. teach a method for making a semiconductor device (figs. 1-3) comprising:

forming a conductive path 13 on a substrate 10, the conductive path made of a first material (Cu) ;

depositing a second material 14 (doped Cu) on the conductive path 13; and

facilitating diffusion of the second material into the conductive path, the second material having a predetermined solubility to substantially diffuse to at least one of an interface and grain boundaries within the first material to significantly increase reliability of the conductive path (col 6, lines 1- 10).

Regarding claim 2, wherein the first material 13 comprises a metal.

Regarding claim 3, wherein the metal is copper (col 5, line 65).

Regarding claim 4, wherein forming the conductive path comprises a damascene process (Fig.1).

Regarding claim 7, further comprising forming a barrier layer 11 between the substrate and the conductive path.

Regarding claim 8, wherein the substrate comprises an interlayer dielectric (ILD) 10.

Regarding claims 9- 10, wherein the second material comprises a noble metal and wherein the second material further comprises at least one of silver, gold, palladium, ruthenium, rhodium, osmium, iridium, and platinum (col 5, line 25-27).

Regarding claim 11, wherein depositing the second material comprises depositing the second material subsequent to a planarization process of the substrate having the conductive path (Fig. 1, col 4, lines 30-35).

Regarding claim 13, wherein depositing the second material comprises depositing the second material before a planarization process of the substrate having the conductive path (col 4, lines 30-35, Fig. 1).

Regarding claim 15, , wherein facilitating diffusion of the second material comprises heat treating the conductive path having the deposited second material (col 5, line 33, Fig. 3).

Regarding claim 16, wherein heat treating the conductive path comprises annealing the conductive path at a predetermined temperature and time to substantially diffuse the second material to the grain boundaries within the first material, the predetermined temperature and time based at least in part on the first and second material (col 5, lines 30-55).

Regarding claim 17. The method of claim 1, wherein the conductive path comprises at least one of a conductive line and a conductive interconnect (Fig. 3).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 9 and 11-17 are rejected under 35 USC 102 (e) as being anticipated by Lopatin et al. (6,624,075).

Lopatin et al. disclose a method for making a semiconductor device comprising: forming a conductive path 26 on a substrate, the conductive path made of a first material; depositing a second material 31 on the conductive path;

Art Unit: 2818

and facilitating diffusion of the second material into the conductive path, the second material having a predetermined solubility (fig. 9) to substantially diffuse to at least one of an interface and grain boundaries within the first material 26 to significantly increase reliability of the conductive path (fig. 2).

Regarding claims 2- 3, wherein the first material 26 comprises a metal and , wherein the metal is copper.

Regarding claim 4, wherein forming the conductive path comprises a damascene process (figs. 1-2).

Regarding claim 5, wherein depositing the second material comprises plating the second material on the conductive path (col 2, lines 40-45).

Regarding claim 6, wherein plating the second material comprises at least one of electroplating, electroless plating, and immersion plating the second material on the conductive path (col 2, lines 40-45).

Regarding claim 7, further comprising forming a barrier layer 10 between the substrate and the conductive path.

Regarding claim 8. The method of claim 1, wherein the substrate comprises an interlayer dielectric (ILD) 8.

Regarding claim 9. The method of claim 1, wherein the second material comprises a noble metal.

Regarding claim 11, wherein depositing the second material comprises depositing the second material subsequent to a planarization process of the substrate having the conductive path (fig. 1).

Regarding claim 12, wherein depositing the second material comprises removing an oxide from the conductive path, and immersing the conductive path in an aqueous solution having at least the second material (col 2, lines 50-55).

Regarding claim 13. The method of claim 1, wherein depositing the second material comprises depositing the second material before a planarization process of the substrate having the conductive path (fig. 1).

Regarding claim 14, wherein depositing the second material comprises removing an oxide from the conductive path, immersing the conductive path in an aqueous solution having at least the second material, and providing a planarization process of the substrate having the conductive path (col 2, lines 50-55).

Regarding claim 15, wherein facilitating diffusion of the second material comprises heat treating the conductive path having the deposited second material (col 5 ,line 65).

Regarding claim 16, wherein heat treating the conductive path comprises annealing the conductive path at a predetermined temperature and time to substantially diffuse the second material to the grain boundaries within the first material, the predetermined temperature and time based at least in part on the first and second material (col 10, lines 45- 55).

Art Unit: 2818

Regarding claim 17, wherein the conductive path comprises at least one of a conductive line and a conductive interconnect (figs. 3- 4).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Art Unit: 2818

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE 
Primary Examiner
Art Unit 2818